REMARKS

Claims 1-32 are pending in the subject application, and are presently under consideration. Claims 1, 8-12 and 18-32 stand rejected. Claims 2-7, 13 - 17 have been indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Rejection of Claims 1, 8-10, 12, 18-19 and 24-32 under 35 U.S.C. 103(a)

Claims 1, 8-10, 12, 18-19 and 24-32 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2002/0129211 to Arimilli ("Arimilli") in view of U.S. Patent No. 6,931,496 to Chen ("Chen"). Applicant traverses this rejection for the following reasons.

Contrary to the assertion in the Office Action regarding claim 1, Arimilli fails to teach that the second node is operative to receive data from the first node and that the second node is operative to assign a shared state to an associated state of the data at the second node. Instead, Arimilli teaches a "system and method for arbitrating between conflicting requests to modify a cache line held in a shared state and for protecting ownership of the cache line granted during such arbitration." See Arimilli, page 7, Par. [0060]. Significantly, nothing on page 7 of Arimilli teaches allowing a second node to receive data from first node and assigning a shared state to an associated state of the data the second node. For example, Arimilli states that if the coherency state associated with the target cache line has a state other than shared or invalid (including a modified state), master 26 simply performs the store into cache array 24 without issuing a transaction on the system bus. Arimilli Par. [0036]. Additionally, master 26 prevents access to the target cache line by other agents 10 by means of appropriate snoop responses until the store into the cache array is completed. Arimilli Par. [0036]. That is, Arimilli focuses on an approach to deal with conflicting requests to modify data that is cached at a plurality of agents in the shared state. Arimilli Abstract. Arimilli does not appear relevant to a second node receiving data from a first node having data in a modified state and assigning a shared state to the data at the second node, as recited in claim 1.

Chen fails to cure the above-noted deficiencies of Arimilli. Additionally, in contrast to the allegations in the Office Action, none of the cited sections of Chen, nor Chen more generally, teach or suggest that a first node is operative to do any action, let alone to provide the data to the second node and transition the associated state of the data at the first node from the modified state to an owner state in response to a non-migratory source broadcast request provided by the second node. For example, the systems and methods of Chen relate to and describe a directory based approach and not a source broadcast protocol. See Col 2, ll. 14 to 25 and Col. 4, ll. 51-55. Thus, the transactions for cached data in Chen, all go through a DSM controller, such that no non-migratory source broadcast request would exist in the system of Chen. Significantly, the DSM controller maintains and manages states of the data (in an associated directory) solely for data in the L3 cache based on the commands issued by the respective processors. Since no non-migratory source broadcast request exists, there consequently can also be no node that would be operative to provide data to the second node in response to such a request.

Moreover, Chen fails to disclose transitioning from a modified state to an owner state in response to the non-migratory source broadcast request, as recited in claim 1. Instead, Chen discloses seven possible states for each of the L3 cache lines: CLEAN, FRESH, DIRTY-ONLY, DIRTY-SHARED, VOID, IDLE. See Chen Col. 4, ll. 60-65. Of these states, only the DIRTY-ONLY and DIRTY-SHARED states indicate that data has been modified. See Chen Col. 5, ll. 6 to 14. Chen fails to teach any command, not even a BRIL command, which enables a second node to receive data from a node with the data in either of the DIRTY-ONLY and DIRTY-SHARED states and set state to a shared state. This is largely because, as discussed above, the approach in Chen employs a DSM controller to handle all requests and the states are not associated with data at more than one node, but instead the states apply to the data in the L3 cache. Another set of different states are used in Chen for a local memory line of the remote node, namely, HOME, SHARED, GONE, and WASH. See Chen Col. 6, ll. 11 to 23.

One of ordinary skill in the art would not expects success to combine the teachings of Chen comprising a Distributed Shared Memory system with the system of Arimilli comprising a central memory system because they would recognize that the transactions required to maintain coherency in a distributed memory system would adversely affect the principal operation of a central memory system (Arimilli System Memory 12). See Chen Fig. 1 and Arimilli Fig 1.

Moreover, the combined teachings still fail to teach or suggest all features recited in claim 1, such that claim 1 would not be obvious to one of ordinary skill in the art in view of Arimilli and Chen.

For these reasons, Applicant respectfully requests reconsideration and allowance of claim 1 and dependent claims 2 to 11.

Regarding claim 8, Chen fails to disclose a source broadcast system so the system is not operative to respond to source broadcasts. Additionally, the approach in Chen does not employ first and second nodes that maintain state and provide responses, as in the system of claim 8. Instead, Chen employs a DSM controller that maintains state and, thus, provides cached data to the respective local processors according to the state of the data in the L3 cache. Significantly, each of the processors in a given node in the system of Chen obtain data via the same DSM controller, such that data is not disclosed as being sent between processors - all requests are through the DSM controller. Reconsideration and allowance of claim 8 are respectfully requested.

Regarding claim 9, in contrast to the allegation in the Office Action, the abstract of Arimilli fails to state that after the first node shares the data to the second node that further migration of the data is precluded when the associated state of the data at the second node is shared data. Instead, the approach in Arimilli protects ownership, but doesn't provide a shared data response and then prevent second node from sharing the data, as is recited in claims 9 and 1 (from which claim 9 depends). Only the first node is permitted to modify or protect data in the first node, which is not the second node sharing the data.

Regarding claim 10, the teaching of Chen at Col. 7, ll. 55 to 61, appears to be unrelated to a non-data response that is provided to the second node. Significantly, Chen fails to teach or suggest a relationship between three nodes: first, second and at least one other node - and also fails to teach a system with source broadcast requests, consistent with what is recited in claim 10. Moreover, in contrast to what appears is being suggested in the Office Action, the commands LRIL or LIL are not responses, but instead are commands issued to read data. Significantly, no responses of any kind are disclosed as being issued by any nodes in the cited section of Chen. Applicant respectfully requests reconsideration and allowance of claim 10.

The Office Action contends claim 12 is unpatentable over the combination of Arimilli in view of Chen by relying on the same rationale used in the rejection of claim 1. We respectfully disagree with this contention. In particular, the grounds use to reject claim 1, being relied on to reject claim 12, fail to present a prima facie case of unpatentability since claim 12 recites features that are not recited in claim 1. As discussed in support of claim 1, Arimilli teaches against providing a shared data response to the second processor node when the associated state of the first processor node cache line being in a modified state. See Arimilli, Par. [0036]. Additionally, as stated in support of claim 1, Chen also fails to teach the transitioning the associated state of the first processor from a modified state to a owner state without updating the memory, as recited in claim 12. Therefore, one of ordinary skill in the art would not be motivated to combine the teaching of Arimilli with the teaching of Chen in order to create the system of claim 1. Accordingly Applicant respectfully requests reconsideration and allowance of claim 12 and its dependant claims 13 to 20.

Claim 18 is further patentable for the reasons discussed above in support of claim 9.

Claim 19 is further patentable for the reasons discussed above in support of claim 12.

Claim 24 is written in means-plus-function format and is patentable for at least the reasons stated above with respect to claim 12. Reconsideration and allowance of claim 24 and claims 25-27 are respectfully requested.

Additionally, claim 25 further recites means for broadcasting a migratory read request and related interactions at the first and second nodes. Claim 25 is patentable for at least the reasons stated above with respect to claim 2.

Regarding claim 26, the Office Action contends that Chen discloses XREADM and XREADN requests. However, as discussed with respect to claim 1, Chen fails to teach the use of any broadcast requests, and FIGS. 4 and 5 fail to demonstrate any use of XREADN and XREADM requests, as suggested in the Office Action. Consequently, claim 26 is patentable.

In addition to Chen failing to teach or suggest any broadcasting of XREADN and XREADM requests, as suggested in the Office Action, the Office Action also fails to demonstrate how Chen might predictively selects the XREADN and XREADN requests, as recited in claim 27. Applicant fails to see the relevance, and the Office Action has not identified

any relevance of FIGS. 4 and 5 to the subject matter recited in claim 27. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 27.

Claim 28 is patentable for at least the reasons stated above with respect to claim 1. Claims 29-31 depend from claim 28 and are therefore also patentable.

Additionally, claim 29 is patentable for at least the reasons stated above with respect to claim 1.

Claim 30 is patentable for at similar reasons to those discussed above with respect to claim 26. For example, Chen does not teach any selection between migratory and non-migratory requests.

Claim 31 s patentable for at least the reasons stated above with respect to claim 27.

Claim 32 is patentable for similar reasons to those stated above with respect to claim 1. Moreover, Chen and Arimilli, taken individually or in combination, fail to distinguish between migratory and non-migratory data requests for the purposes of allowing and preventing further migration of data to cache associated with the source processor node, as recited in claim 32. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 32.

II. Rejection of Claims 11 and 20-23 under 35 U.S.C. 103(a)

Claims 11 and 20-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Chen and further in view of U.S. Patent No. 6,484,240 to Cypher ("Cypher"). Applicant traverses this rejection for the following reasons.

Claim 11, depends from claim 1 and is patentable over the identified combination of references since Cypher fails to cure the deficiencies of Arimilli and Chen as discussed *supra*. Moreover, Chen and Arimilli do not teach how the second cache controller is effecting state transitions associated with the data based upon data request and responses for the associated cache of the second processor. Instead, in Chen, the DSM controller is not associated with a given processor, but provides shared access to data in L3 cache that is utilized by each processor in the respective node. Thus, the line of data in the L3 cache has only one state - the state provided by the DMS controller. In view of the divergent teachings between the respective

references, Applicant fails to see one of ordinary skill in the art would try to combine these references. It is unclear how a system implementing a source broadcast request with a moving CDP (Arimilli) would be combined with a system with that implements fixed DSM to control a distributed memory (Chen) and would further be combined with the protocol and methods taught by Cypher. Reconsideration and allowance of claim 11 are respectfully requested.

The Office Action contends that Claim 21 is unpatentable over Arimilli, in view of Chen and further in view of Cypher by incorporating the rational of used in rejecting claim 1 and 11. Applicant respectfully disagrees with this contention. Claim 11, which depends from claim 1, should be allowable for the reasons stated in support of claim 1. Moreover, the Addition of Cypher fails to cure the deficiencies of Arimilli in view of Chen relative to both claim 1 and claim 21. For example the combination of Arimilli, Chen and Cypher fail to teach or suggest providing a shared data response to the source processor and by transitioning the associated state of the target processor from a modified state to an owner state without updating memory. Accordingly, applicant respectfully requests reconsideration and allowance of claim 21.

Claims 22 and 23 are patentable for at least the reasons claim 21 is patentable and for the specific features recited therein. Moreover, Chen fails to teach or suggest the use of an S-data and D-data response, as recited in claims 22 and 23, respectively. Instead, as discussed above, responses in Chen are not from processors, but instead originate with the DSM controller. Accordingly, claims 22 and 23 are patentable, and their allowance is respectfully requested.

III. Allowable Subject Matter

Applicant appreciates the indication that claims 2-7, 13-17 contain allowable subject matter.

IV. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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